Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-10 (previously cancelled)

Claim 11 (Previously presented): A gain circuit, comprising:

a substrate;

a first differential pair amplifier disposed upon the substrate and coupled to a first circuit output having a gain contributing to circuit gain in direct proportion to the first differential pair amplifier gain;

a second differential pair amplifier disposed upon the substrate and coupled to a second circuit output having a gain, and coupled to the first differential amplifier such that an increase in second differential pair amplifier gain contributes to a decrease in the circuit gain; and

a variable voltage source coupled to the circuit outputs, a voltage output of the variable voltage source determining respective drain source voltages on the first differential pair and the second differential pair based on a differential input signal received at the first differential pair amplifier and the second differential pair amplifier, and thereby controlling the gain of the first differential pair and the gain of the second differential pair,

wherein the variable voltage source controls a transconductance of the gain circuit so as to improve linearity of the gain circuit.

Claim 12 (original): The gain circuit of claim 11, wherein the first differential pair amplifier includes:

a first transistor; and

a second transistor,

wherein the variable voltage source controls a transconductance of the first transistor so as to flatten a transconductance transfer characteristic of the first transistor; and

wherein the variable voltage source controls a transconductance of the second transistor so as to flatten a transconductance transfer characteristic of the second transistor.

Claim 13 (original): The gain circuit of claim 11, wherein the second differential pair amplifier includes:

a first transistor; and

a second transistor,

wherein the variable voltage source controls a transconductance of the first transistor so as to flatten a transconductance transfer characteristic of the first transistor; and

wherein the variable voltage source controls a transconductance of the second transistor so as to flatten a transconductance transfer characteristic of the second transistor.

Claim 14 (original): The gain circuit of claim 11, wherein:

the first differential pair amplifier includes

a first transistor; and

a second transistor,

wherein the variable voltage source controls a transconductance of the first transistor so as to flatten a transconductance transfer characteristic of the first transistor; and

wherein the variable voltage source controls a transconductance of the second transistor so as to flatten a transconductance transfer characteristic of the second transistor; and

the second differential pair amplifier includes

a third transistor; and

a fourth transistor,

wherein the variable voltage source controls a transconductance of the third transistor so as to flatten a transconductance transfer characteristic of the third transistor; and

wherein the variable voltage source controls a transconductance of the fourth transistor so as to flatten a transconductance transfer characteristic of the fourth transistor.

Claim 15 (Previously presented): The gain circuit of claim 14, wherein drain source voltages of the first, second, third, and fourth transistors are adjusted so as to flatten corresponding transfer characteristics of the first, second, third, and fourth transistors.

Claim 16 (original): The gain circuit of claim 15, wherein the drain source voltages across the first, second, third, and fourth transistors are reduced upon reducing a DC voltage at the output of the first and second differential pairs.

Claim 17 (original): The gain circuit of claim 15, wherein the transconductance transfer characteristic of each of the first, second, third, and fourth transistors is a relationship between the transconductance of the transistor versus a gate source voltage of the transistor as the drain source voltage across the transistor is varied.

Claim 18 (Currently amended): A method for providing, over a wide range of input signal voltages, variable gain amplification having a linear change in output current gain at a differential current output port as a function of a change in differential voltage input at a differential voltage input port, the variable gain amplification provided by a variable gain amplifier responsive to the differential voltage input, the method comprising the steps of:

receiving an input signal voltage; and

~~generating a voltage control signal based on an amplitude of the input signal voltage; and~~

adjusting a transconductance of the variable gain amplifier in response to the ~~voltage control signal~~ input signal voltage so as to flatten a transconductance transfer characteristic of the variable gain amplifier, the adjusting step including reducing a drain source voltage across the variable gain amplifier for increasing amplitude of the input signal voltage.

Claim 19 (original): The method of claim 18, wherein the adjusting step includes the steps of:

adjusting a transconductance of a first common source differential pair amplifier of the variable gain amplifier so as to flatten a transconductance transfer characteristic of the first common source differential pair amplifier; and

adjusting a transconductance of a second common source differential pair amplifier of the variable gain amplifier so as to flatten a transconductance transfer characteristic of the second common source differential pair amplifier.

Claim 20 (original): The method of claim 19, wherein the adjusting a transconductance of the first common source differential pair amplifier includes the steps of:

adjusting a transconductance of a first transistor so as to flatten a transconductance characteristic of the first transistor; and

adjusting a transconductance of a second transistor so as to flatten a transconductance characteristic of the second transistor,

wherein the first and second transistor share a common source and are connected to form the first common source differential pair amplifier.

Claim 21 (original): The method of claim 19, wherein the adjusting a transconductance of the second common source differential pair amplifier includes the steps of:

adjusting a transconductance of a first transistor so as to flatten a transconductance characteristic of the first transistor; and

adjusting a transconductance of a second transistor so as to flatten a transconductance characteristic of the second transistor,

wherein the first and second transistor share a common source and are connected to form the second common source differential pair amplifier.

Claim 22 (original): The method of claim 18, wherein the adjusting step includes the steps of:

adjusting a transconductance of a first transistor so as to flatten a transconductance characteristic of the first transistor;

adjusting a transconductance of a second transistor so as to flatten a transconductance characteristic of the second transistor;

adjusting a transconductance of a third transistor so as to flatten a transconductance characteristic of the third transistor; and

adjusting a transconductance of a fourth transistor so as to flatten a transconductance characteristic of the fourth transistor,

wherein the first and second transistor share a common source and are connected to form a first common source differential pair amplifier of the variable gain amplifier; and

wherein the third and fourth transistor share a common source and are connected to form a second common source differential pair amplifier of the variable gain amplifier.

Claim 23 (original): The method of claim 22, wherein the adjusting a transconductance of the first, second, third, and fourth transistor steps each include the step of:

reducing a drain source voltage across the corresponding first, second, third, or fourth transistor.

Claim 24 (cancelled)

Claim 25 (Currently amended): The method of claim 23, wherein the drain source voltages across corresponding first, second, third, and fourth transistors are reduced by reducing a variable DC voltage applied at the differential current output port ~~in response to the voltage control signal~~.

Claim 26 (original): The method of claim 23, wherein the transconductance transfer characteristic of the corresponding first, second, third, or fourth transistor is a relationship between the transconductance of the corresponding transistor versus a gate source voltage of the corresponding transistor as the drain source voltage across the corresponding transistor is varied.